DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

PhD Qualifier Examination, Paper II

Total time: 2 Hours **October 30, 2009** **Maximum Marks: 120**

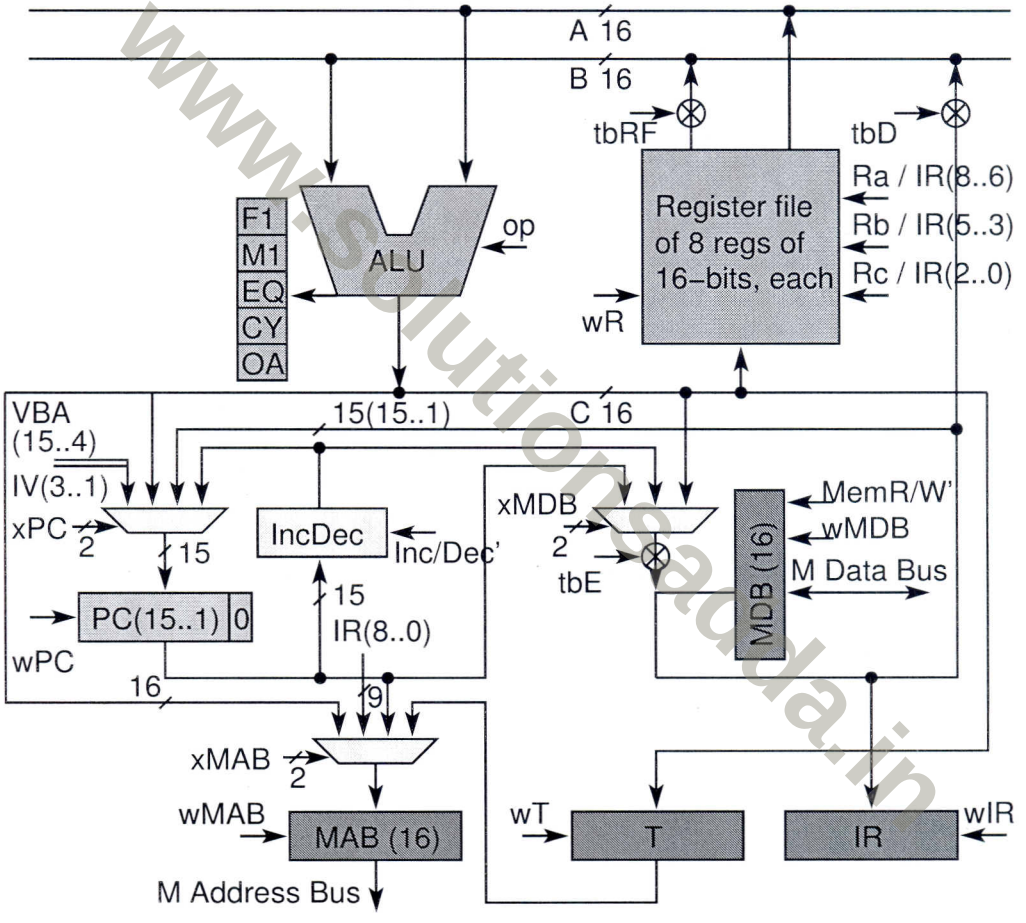
Answer from ALL the three parts

Part A: Computer Organisation and Architecture

Answer FOUR questions in this part

1. Perform a shift-and-add multiplication on the 2's complement representation of -5 and -2 in 4 bits to obtain the correct result. 10

2. Consider the CPU in the given figure.



tbX: tristate output of X to bus (eg. tbD); wX: write/latch to X (eg. wIR, wMDB)
MemR/W'=1:Data from Mem to bus; MemR/W'=0: Data from bus to Mem
xMUX: select input of MUX; IV: interrupt vector; VBA: vector base address
F1, M1, EQ, CY,OA: various flags set depending on ALU operation and output

The `LDM R M` instruction for loading register `R` (indicated as `rrr`) with the contents of the memory location `M` consists of the main instruction as `1110000rrr------` followed by a 16-bit address.

Ignoring details in the data path not relevant to this instruction, list the micro-operations, wrt the given data path, to carry out `LDM R M`, beyond fetching the first instruction word. 10

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3. Consider a memory hierarchy with two-level cache and main memory with the following parameters:

   L1 cache: access time of 2 ns, hit ratio of 90%
   L2 cache: access time of 10 ns, hit ratio of 95%
   Main memory: access time of 100 ns

   Estimate the average access time for a read operation, assuming that if a data item is not found in a particular level, it can be directly accessed from the next level (i.e. calculations for block transfer overheads can be ignored). 10

4. Consider a synchronous k-stage pipeline with stage delays $T_1, T_2, \ldots, T_k$. There are registers placed between adjacent stages, each of delay T_R. Estimate the total time required to process m inputs sets in the pipeline. 10

5. Answer the following on the operation of DMA:

   i) Draw the schematic diagram of a DMA controller indicating its connections to the CPU, peripherals and the memory. 5

   ii) Explain the basic steps in the operation of a DMA controller, with respect to your diagram. 5

Part B: Operating Systems

Answer ALL questions in this part

1. A 16-bit computer has a page size of 1024 bytes. The page table of a process is as follows:

Page no.	Frame no.
0	7
1	2
2	5
3	1
4	12
5	6
6	6
7	0

   Determine the physical addresses corresponding to the logical addresses: *i*) 3720 and *ii*) 11225 8

2. In the context of virtual memory, what is Belady's anomaly and how does it happen? 4

3. Consider the following snap-shot of processes to be executed using round robin algorithm with a time slice of 1 ms. Determine the average turnaround time for the processes. Ignore the context switching time. 12

Process	Execution time (ms)	Arrival time (ms)
P_1	4	0
P_2	5	2
P_3	6	5
P_4	2	6

4. In a typical process state transition diagram, clearly state under what conditions the following state transitions occur:

   i) Running to Ready 2

   ii) Running to Blocked (Waiting) 2

   iii) Blocked (Waiting) to Ready 2

5. Answer the following questions on semaphores:

   i) Define a semaphore. 3

   ii) Give the outline of a program to fork two process, one to print in ascending order (AO) only even numbers in the range 1..100 and the other to print in AO only odd numbers in the range 1..100; the two process should be synchronised so that the resulting output is the sequence of numbers in the range 1..100 in AO (so that the two two processes print alternatingly). 7

Part C: Programming

Answer ALL questions in this part

1. Write code for the following in 'C':

   i) type definition to represent a node of a binary tree 4

   ii) a function to count the number of nodes in a given binary tree 6

   iii) a function to search for an integer in a given binary search tree 8

2. Write code for the following in 'C':

   i) type definition to (approximately) represent a point in 2-D real space 2

   ii) type definition to represent a line segment in 2-D real space using the the defined points 2

   iii) type definition to represent a triangle in 2-D real space 3

   iv) a function that takes a triangle and a line segment and returns true if the line segment intersects the triangle and false otherwise 15